WHAT IS CLAIMED IS:

1. A driving circuit comprising:

a first amplifier circuit for charging and driving an output terminal of said driving circuit;

a second amplifier circuit for discharging and driving said output terminal;

said first and second amplifier circuits having respectively first and second operating ranges overlapping at least in part each other; and

an input control circuit receiving a first voltage located at a lower limit side of an overlapped portion between the first operating range and the second operating range, a second voltage located at an upper limit side of the overlapped portion, and a target voltage, for selecting at least one of the received voltages to supply the selected voltage to an input terminal of said first amplifier circuit and/or an input terminal of said second amplifier circuit;

a driving period for driving said output terminal to the target voltage being made up by at least a first period and a second period;

said input control circuit performing control so that during the first period, one of the first voltage and the second voltage, is supplied in common to said input terminals of said first amplifier circuit and said second amplifier circuit, or the first and second voltages are respectively supplied to said input terminal of said first amplifier circuit and said input terminal of said second amplifier circuit, and

during the second period, the target voltage is supplied in common to said input terminals of said first amplifier circuit and said

second amplifier circuit.

2. The driving circuit according to claim 1, wherein said input control circuit supplies either of the first voltage and the second voltage to said input terminals of said first amplifier circuit and said second amplifier circuit in common during the first period.

3. The driving circuit according to claim 1, wherein said input control circuit supplies the first voltage and the second voltage to said input terminal of said first amplifier circuit and said input terminal of said second amplifier circuit, respectively.

4. The driving circuit according to claim 1, wherein said first amplifier circuit and said second amplifier circuit are both of a voltage follower configuration; and wherein

during the first period, said input control circuit supplies the second voltage to said input terminals of said first amplifier circuit and said second amplifier circuit in common when the target voltage is equal to or more than a predetermined reference voltage within the overlapped portion between the first operating range and the second operating range, and

supplies the first voltage to said input terminals of said amplifier circuit and said second amplifier circuit in common when the target voltage is less than the reference voltage.

5. The driving circuit according to claim 1, further comprising

a switch connected between an input terminal from which said input control circuit receives said target voltage and said output terminal.

6. The driving circuit according to claim 1, wherein said first amplifier circuit comprises:

a first differential pair of a first polarity having first and second input terminals, for differentially receiving input signal voltages from said first and second input terminals; and

a first transistor connected between a first power supply and said output terminal, and having a control terminal coupled to an output of said first differential pair; and wherein

said second amplifier circuit comprises:

a second differential pair of a second polarity having first and second input terminals, for differentially receiving input signal voltages from said first and second input terminals; and

a second transistor connected between a second power supply and said output terminal, and having a control terminal coupled to an output of said second differential pair.

7. The driving circuit according to claim 1, wherein said first amplifier circuit comprises:

a first differential pair of a first polarity having first and second input terminals, for differentially receiving input signal voltages from said first and second input terminals; and

a first transistor connected between a first power supply and said output terminal, and having a control terminal coupled to an output of said first differential pair;

wherein

said second amplifier circuit comprises:

a second differential pair of a second polarity having first and second input terminals, for differentially receiving the input signal voltages from said first and second input terminals; and

a second transistor connected between a second power supply and said output terminal, and having a control terminal coupled to an output of said second differential pair;

said first input terminals of said first and second differential pairs being connected in common; and

wherein

said input control circuit comprises first through third switches having one terminals for receiving the first voltage, the second voltage and the target voltage, respectively; the other terminals of said first through third switches being connected in common to said commonly coupled first input terminals of said first and second differential pairs.

8. The driving circuit according to claim 1, wherein said first amplifier circuit comprises:

a first differential pair of a first polarity having first and second input terminals, for differentially receiving input signal voltages from said first and second input terminals; and

a first transistor connected between a first power supply and said output terminal, and having a control terminal coupled to an output of said first differential pair;

wherein

said second amplifier circuit comprises:

a second differential pair of a second polarity having first and

second input terminals, for differentially receiving the input signal voltages from said first and second input terminals; and

a second transistor connected between a second power supply and said output terminal, and having a control terminal coupled to an output of said second differential pair; and

wherein

said input control circuit comprises:

first and second switches having one terminals for receiving the first voltage and the second voltage, respectively; and

third and fourth switches having one terminals for receiving the target voltage in common;

the other terminals of said first and third switches being connected in common to said first input terminal of said first differential pair; and the other terminals of said second and fourth switches being connected in common to said first input terminal of said second differential pair.

9. The driving circuit according to claim 6, wherein in each of said first and second amplifier circuits,

said first input terminals of said first and second differential pairs constitute non-inverting input terminals, and

said second input terminals of said first and second differential pairs constitute inverting input terminals and are connected to said output terminal.

10. The driving circuit according to claim 7, wherein said first through third switches adapted to be turned on/off, respectively, by a

control signal are controlled so that

during the first period, said first or second switch is turned on, while said third switch is turned off; and

during the second period, said third switch is turned on, while said first and second switches are turned off.

11. The driving circuit according to claim 8, wherein said first through fourth switches adapted to be turned on/off, respectively, by a control signal are controlled so that

during the first period, said first and second switches are turned on, while said third and fourth switches are turned off; and

during the second period, said third and fourth switches are turned on, while said first and second switches are turned off.

12. The driving circuit according to claim 1, wherein said first amplifier circuit comprises:

a first current source connected to a second power supply;

a first differential pair of a first polarity being driven by said first current source and having a non-inverting input terminal and an inverting input terminal, said first differential pair differentially receiving input signal voltages from said non-inverting input terminal and said inverting input terminal thereof;

a first load circuit connected between a pair of outputs of said first differential pair and a first power supply; and

a first transistor being connected between said first power supply and said output terminal, and having a control terminal coupled to the output of said first differential pair;

wherein

said second amplifier circuit comprises:

a second current source connected to said first power supply;

a second differential pair of a second polarity, being driven by said second current source and having a non-inverting input terminal and an inverting input terminal, said second differential pair differentially receiving the input signal voltages from said non-inverting input terminal and said inverting input terminal thereof;

a second load circuit connected between a pair of outputs of said second differential pair and said second power supply; and

a second transistor being connected between said second power supply and said output terminal, and having a control terminal coupled to the output of said second differential pair;

said respective inverting input terminals of said first and second differential circuits being connected to said output terminal;

wherein

said input control circuit comprises first through third switches having one terminals for receiving the first voltage, the second voltage, and the target voltage, respectively;

the other terminals of said first through third switches being connected in common to said commonly coupled non-inverting input terminals of said first and second amplifier circuits;

wherein

said first amplifier circuit further comprises:

a third current source and a fourth switch connected in series

between said second power supply and said output terminal; and

wherein

said second amplifier circuit further comprises:

a fourth current source and a fifth switch, connected in series between said first power supply and said output terminal.

13. The driving circuit according to claim 1, wherein said first amplifier circuit comprises:

a first current source connected to a second power supply;

a first differential pair of a first polarity driven by said first current source and having a non-inverting input terminal and an inverting input terminal, said first differential pair differentially receiving input signal voltages from said non-inverting input terminal and said inverting input terminal thereof;

a first load circuit connected between a pair of outputs of said first differential pair and a first power supply; and

a first transistor being connected between said first power supply and said output terminal, and having a control terminal coupled to the output of said first differential pair;

wherein

said second amplifier circuit comprises:

a second current source connected to said first power supply;

a second differential pair of a second polarity, driven by said second current source and having a non-inverting input terminal and an inverting input terminal, said second differential pair differentially receiving the input signal voltages from said non-inverting input

terminal and said inverting input terminal thereof;

a second load circuit connected between a pair of outputs of said differential pair and said second power supply; and

a second transistor being connected between said second power supply and said output terminal, and having a control terminal coupled to the output of said second differential pair;

said respective inverting input terminals of said first and second differential circuits being connected to said output terminal;

wherein

said input control circuit comprises:

first and second switches having one terminals for receiving the first voltage and the second voltage respectively; and

third and fourth switches having one terminals for receiving the target voltage in common;

the other terminals of said first and third switches being connected in common to said non-inverting input terminal of said first amplifier circuit;

the other terminals of said second and fourth switches being connected in common to said non-inverting input terminal of said second amplifier circuit;

wherein

said first amplifier circuit further comprises:

a third current source and a fifth switch connected in series between said second power supply and said output terminal; and

wherein

said second amplifier circuit further comprises:

a fourth current source and a sixth switch, connected in series between said first power supply and said output terminal.

14. The driving circuit according to claim 12, wherein said first through fifth switches adapted to be turned on or off, respectively, by a control signal are controlled so that;

during the first period, said first or second switch is turned on, said third switch is turned off, and said fourth and fifth switches are turned off; and

during the second period, said third switch is turned on, said first and second switches are turned off, and one of said fourth and fifth switches is turned on.

15. The driving circuit according to claim 13, wherein said first through sixth switches adapted to be turned on or off, respectively, by a control signal are controlled so that

during the first period, said first and second switches are turned on, said third and fourth switches are turned off, and said fifth and sixth switches are turned off; and

during the second period, said third and fourth switches are turned on, said first and second switches are turned off, and one of said fifth and sixth switches is turned on.

16. The driving circuit according to claim 1, wherein said first and second amplifier circuits are of a voltage follower configuration.

17. The driving circuit according to claim 1, further comprising:

a switch connected between an input terminal from which said

input control circuit receives said target voltage and said output terminal:

wherein said driving period for driving said output terminal to the target voltage further comprises a third period after the first period and the second period; and

during the third period, said switch connected between said input terminal and said output terminal is turned on.

18. The driving circuit according to claim 1, wherein a lower limit and an upper limit of the first operating range are defined by a first threshold voltage defining the lower limit of the operating range of said first amplifier circuit and a high-potential power supply voltage, respectively;

wherein

an upper limit and a lower limit of the second operating range are defined by a second threshold voltage defining the upper limit of the operating range of said second amplifier circuit and a low-potential power supply voltage, respectively; and

wherein

the first voltage is set to be equal to or more than the first threshold voltage; and

the second voltage is set to be higher than the first voltage and equal to or less than the high-power potential power supply voltage minus said second threshold voltage.

19. A driving circuit having an input terminal and an output terminal and outputting an output signal from said output terminal responsive to a

signal voltage supplied to said input terminal, said driving circuit comprising:

an amplifier circuit for charging and/or discharging and driving a capacitive load connected to said output terminal, based on the voltage at said input terminal; and

an input control circuit for performing control so that a predetermined constant voltage within an operating range of said amplifier circuit and the signal voltage supplied to said input terminal are switched for supply to an input terminal of said amplifier circuit.

20. The driving circuit according to claim 19, wherein a driving period for driving said output terminal includes at least a first period and a second period; and wherein

said input control circuit performs switching control so that the predetermined constant voltage is supplied to said input terminal of said amplifier circuit during the first period, and

the input signal voltage supplied to said input terminal is supplied to said input terminal of said amplifier circuit during the second period.

21. The driving circuit according to claim 19, wherein said amplifier circuit includes:

a first amplifier circuit for charging and driving said output terminal; and

a second amplifier circuit for discharging and driving said output terminal;

said first and second amplifier circuits having respectively first and second operating ranges overlapping at least in part each other;

wherein

said input control circuit performs control so that at least one selected among a voltage located at a lower limit side of an overlapped portion between the first operating range and the second operating range (referred to as a "first voltage"), a voltage located at an upper limit side of the overlapped portion (referred to as a "second voltage"), and a target voltage supplied to said input terminal is supplied to an input terminal of said first amplifier circuit and/or an input terminal of said second amplifier circuit;

a driving period for driving said output terminal to the target voltage including at least a first period and a second period;

said input control circuit performing control so that during the first period, one selected between the first voltage and the second voltage is supplied in common to said input terminals of said first amplifier circuit and said second amplifier circuit, or the first voltage and the second voltage are supplied to said input terminal of said first amplifier circuit and said input terminal of said second amplifier circuit, respectively, and

during the second period, the target voltage is supplied in common to said input terminals of said first amplifier circuit and said second amplifier circuit.

22. A display device comprising:

a plurality of data lines for supplying image signals to pixels on a display unit; and

a driving circuit as set forth in claim 1, for driving said data

lines.

23. The driving circuit according to claim 7, wherein in each of said first and second amplifier circuits,

said first input terminals of said first and second differential pairs constitute non-inverting input terminals, and

said second input terminals of said first and second differential pairs constitute inverting input terminals and are connected to said output terminal.

24. The driving circuit according to claim 8, wherein in each of said first and second amplifier circuits,

said first input terminals of said first and second differential pairs constitute non-inverting input terminals, and

said second input terminals of said first and second differential pairs constitute inverting input terminals and are connected to said output terminal.